LSD Lab 2011

Submission deadline MON 9 September, 2011. 12 night. Complete assessment on TUE Sept 10 ,2011 during lab time.
Following circuits are to be described and simulated and tested. What is to be done is briefly described against each circuit.
(These should be kept in the library for future use)

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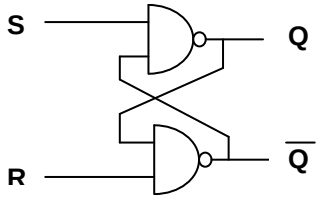
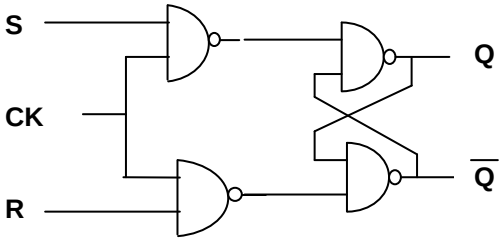
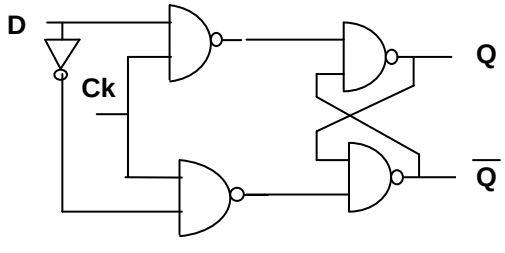
1. Basic Memory Element
Programs for Structural and behavioral description using process and test them to see that the transition table is implemented.



2. SR LATCH
Programs for Structural and behavioral description using process and test them to see that the transition table is implemented.
Also vary clock width and test for values of S and R changing, when CK is high.



3. D Latch
Programs for Structural and behavioral description using process and test them to see that the transition table is implemented.
Also vary clock width and test for values of S and R changing, when CK is high.



4 EXPT ON JK FLIP-FLOPS AND IT ITS USE

(At the end of this experiment we need with you all working Flip-flops which could be used as components in future labs. We should avoid multiple commands given at the same time to a ciruit. (Here clear, preset and CK are three different commands, so should not be given at the same time Only one should be active at a time).

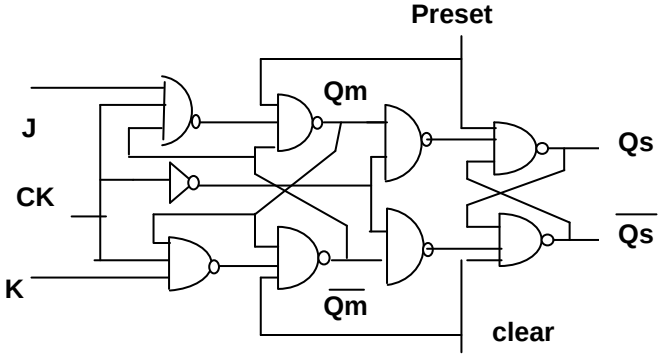
5. EXPT ON JK FLIP_FLOPS

Describe the Master slave flip-flop below using structural and behavioral description (should depict internal master slave behaviour) using process. Testing should check up

1.1. Preset and clear o clock signal actions. Ie. Check Preset and clear has overriding effect or not irrespective of clock being active and what ever may be JK values. Test data thus must have various values to the signals so as to demo the outputs.

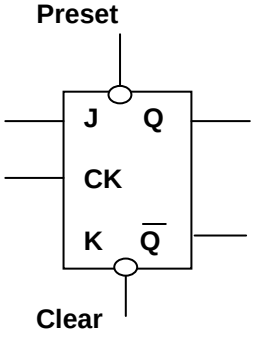
1.2. Demo what happens when both Preset and clear are active and then released to 1. with clock active and inactive.

1.3. Show the clock action (Preset/clear are inactive) for various J K values. i.e., Demo the transition table of JK latch.



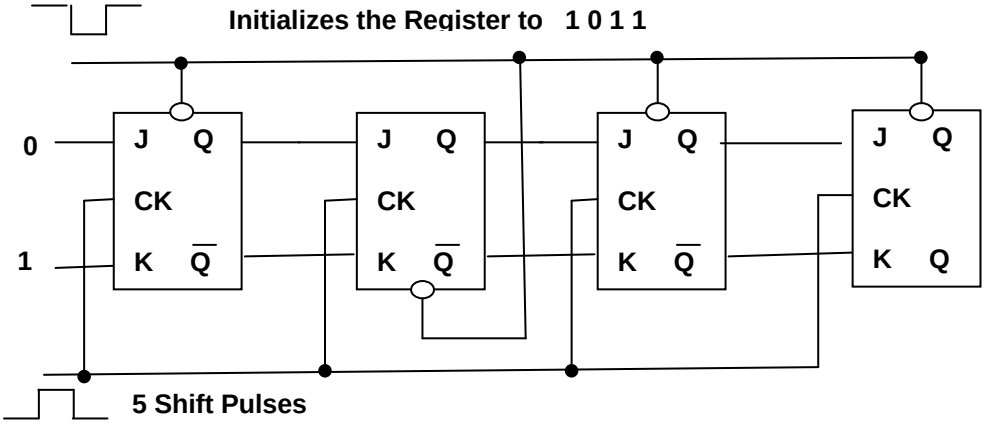
Transition Table

J	K	Q_n
0	0	Q_{old}
0	1	0
1	0	1
1	1	$\overline{Q}_{old}$



6. 4-BIT SHIFT REGISTER USING JK LATCHES

Construct the 4 bit shift register(using structural description with JK flip-flop as compoenent from 1) . Demonstrate proper functioning irrespective of clock width. Show proper function for each clock for 5 clock pulses.



synchronous FSM

7. Draw a state diagram and give a minimized state table and its logic circuit implementation for a machine that outputs z= 1 immediately after encountering a block of odd 1s in the input.
   Example input /output below:
   X = 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0
   Z= 0 0 0 1 0 1 0 0 0 1 0 0 0 10 1 0

ASYNCHRONOUS FSM

8. Find the minimal =closed cover for the following incompletely specified machine and give it reduced flow table. Implement the same. Give the output sequences for the input sequences below using the state table and also the implemented logic circuit circuit.
   X1= 11111110000000101010111010 10
   X2 = 00000101010101010111010101010

Flow table

PS	NS, z x_1x_2 00	01	11	10
A	- , -	C , 1	E, 1	B, 1
B	E, 0	- , -	-, -	-, -
C	F, 0	F, 1	-, -	-,-
D	-. -	-, -	B, 1	-, -
E	-, -	F, 0	A, 0	D, 1
F	C, 0	- , -	B, 0	C, 1